



The Need for New AI Processor Power Delivery

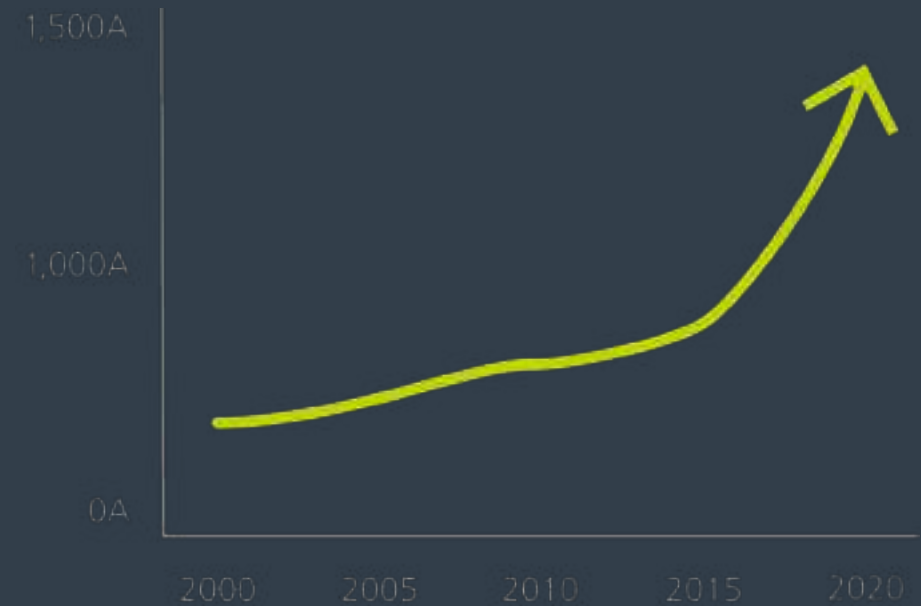
Robert Gendron, P.E.
Corporate Vice President, Vicor

AI Hardware Summit
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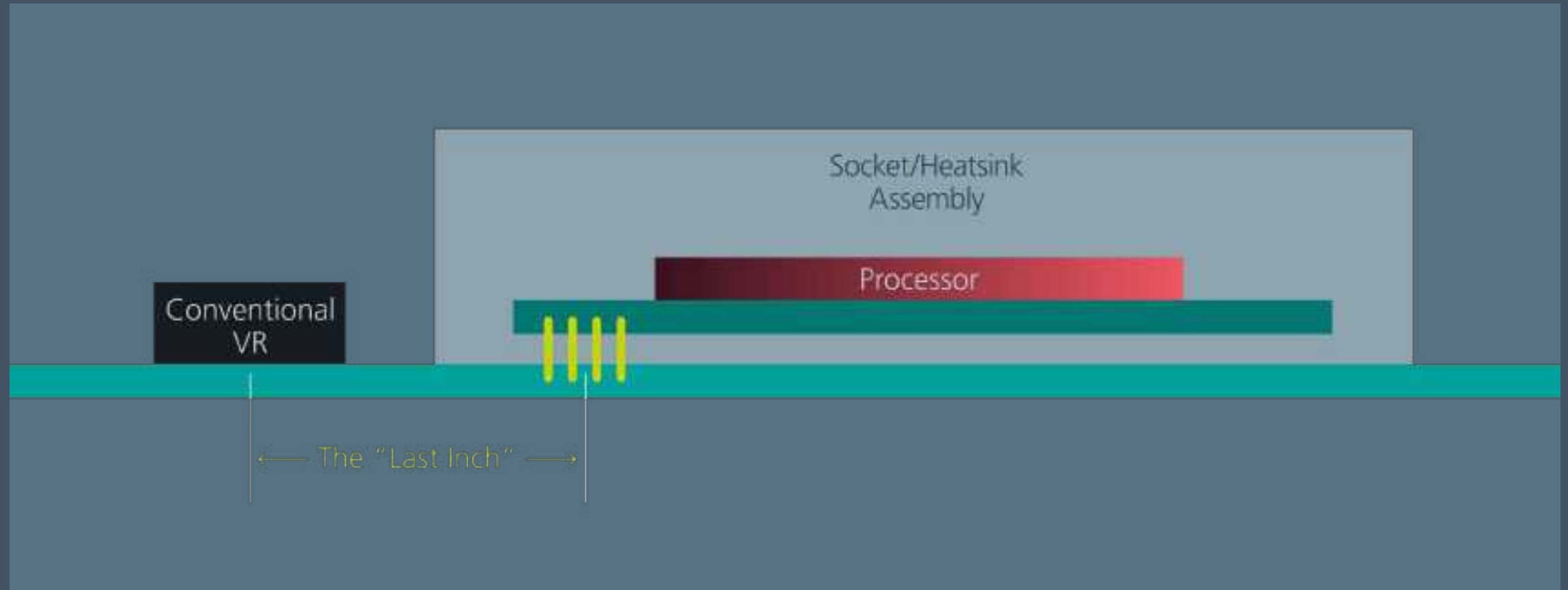
Challenge in powering AI processors

- AI processors need a lot of current...
- Decreases in power efficiency
 - increasing PDN distribution losses
- Significant operating performance reduction if power demands are not met

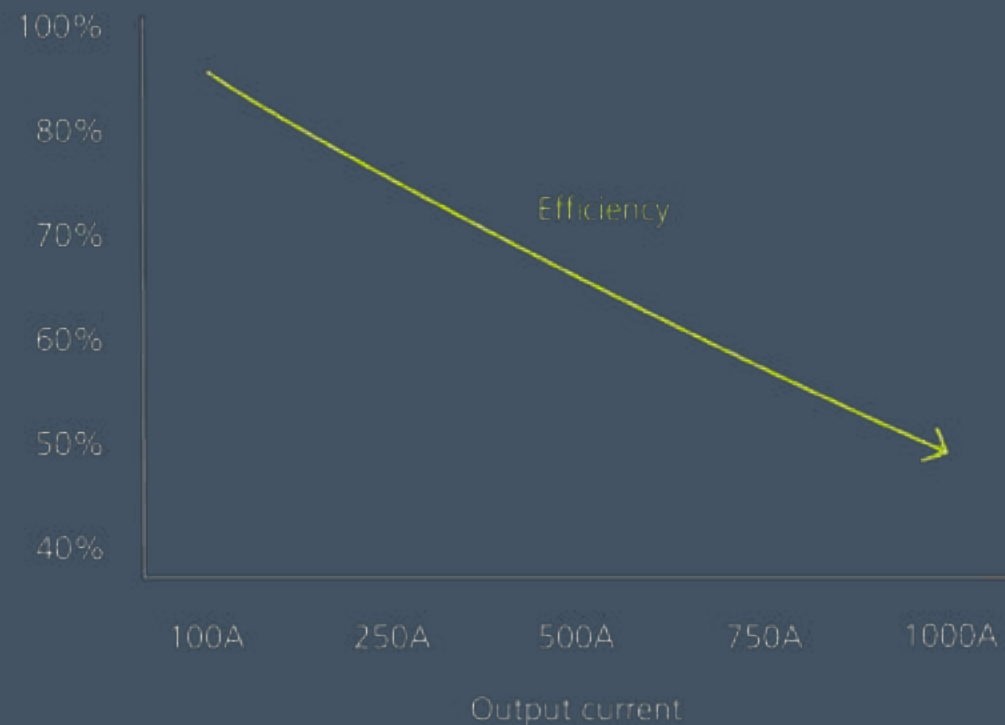
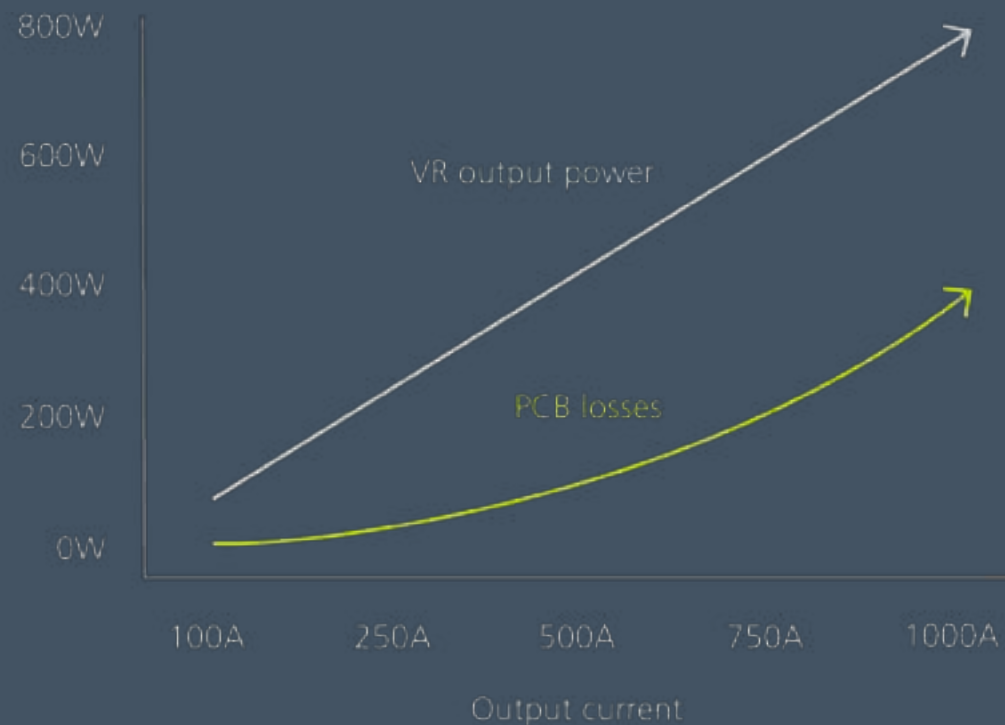
Progression of CPU/GPU/ASIC/FPGA peak current requirements



The “last inch”



VR to the processor losses, the “last inch”



Example with PCB resistance of 400uOhm (VR at 0.8Vout)

Conventional multiphase

- Conversion performed by DrMOS/Inductor
- High conversion ratio (minimum 12:1)
- Challenging to scale for higher currents
- Phase imbalancing
- Noise generation
- Size prohibits reducing PDN

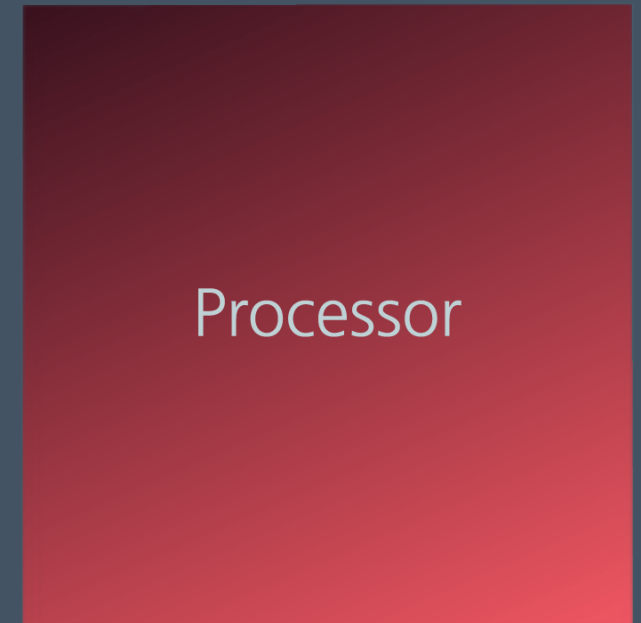


Factorized Power Architecture

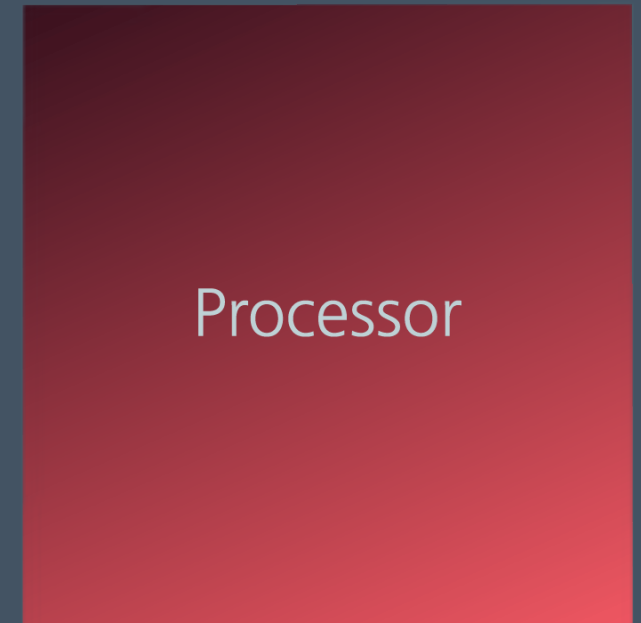
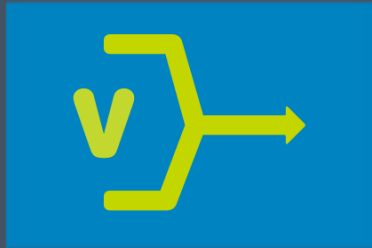


- Regulation followed by transformation
- Allows for optimization of each function
- Enables re-distribution of power
- High density
- Low noise

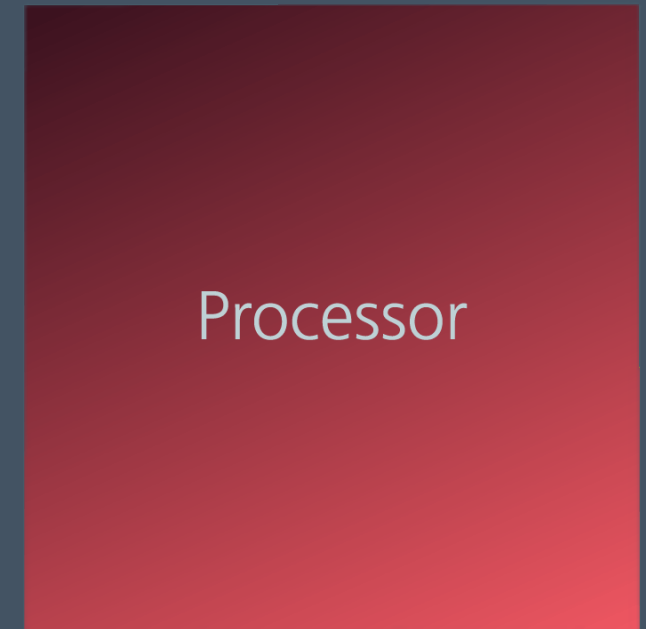
Factorized Power Architecture



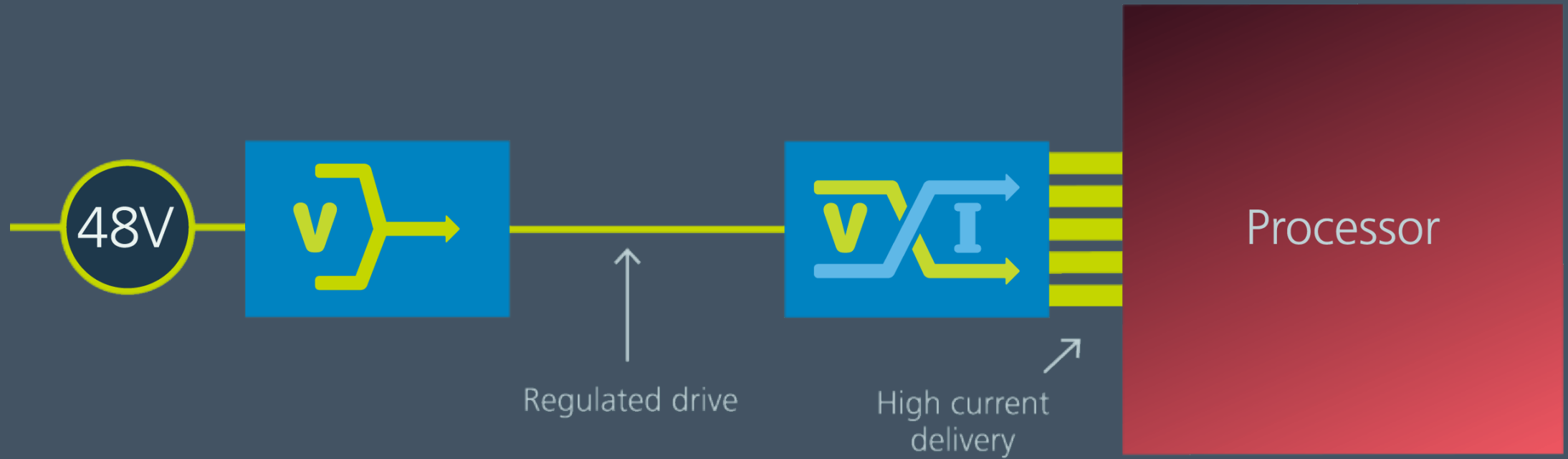
Factorized Power Architecture



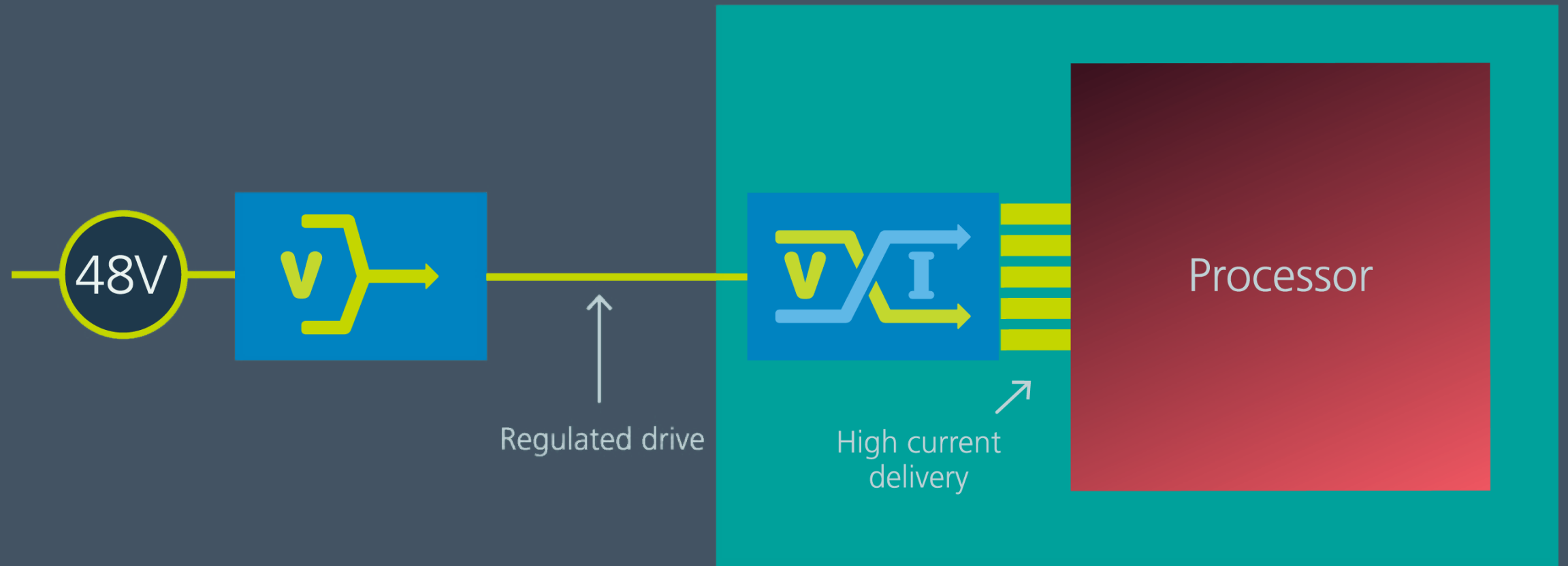
Factorized Power Architecture



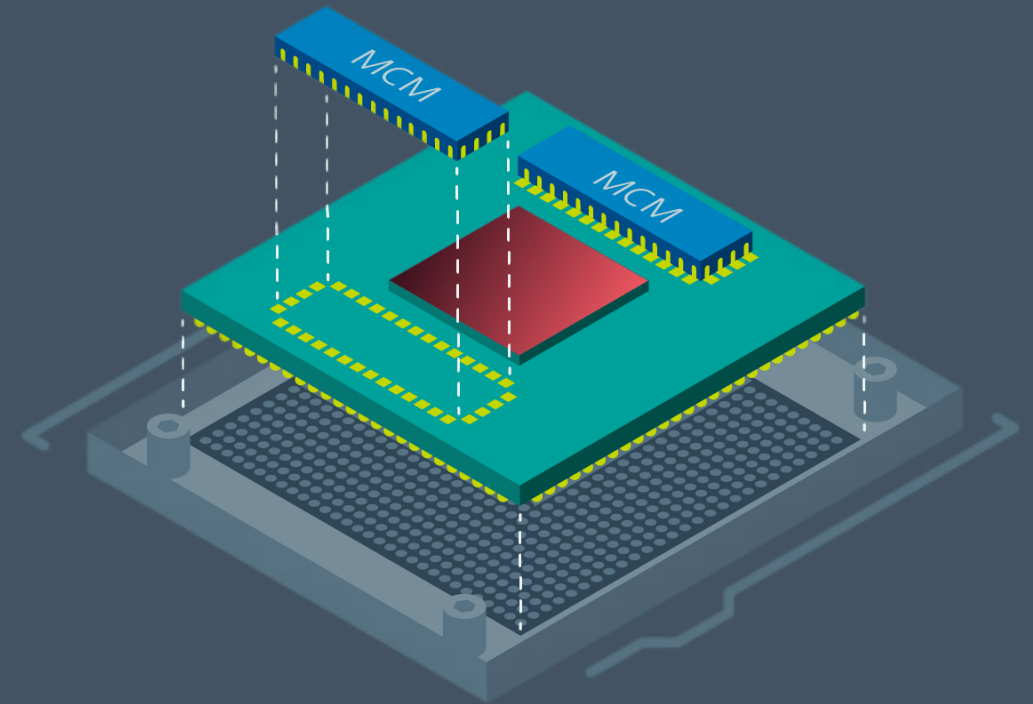
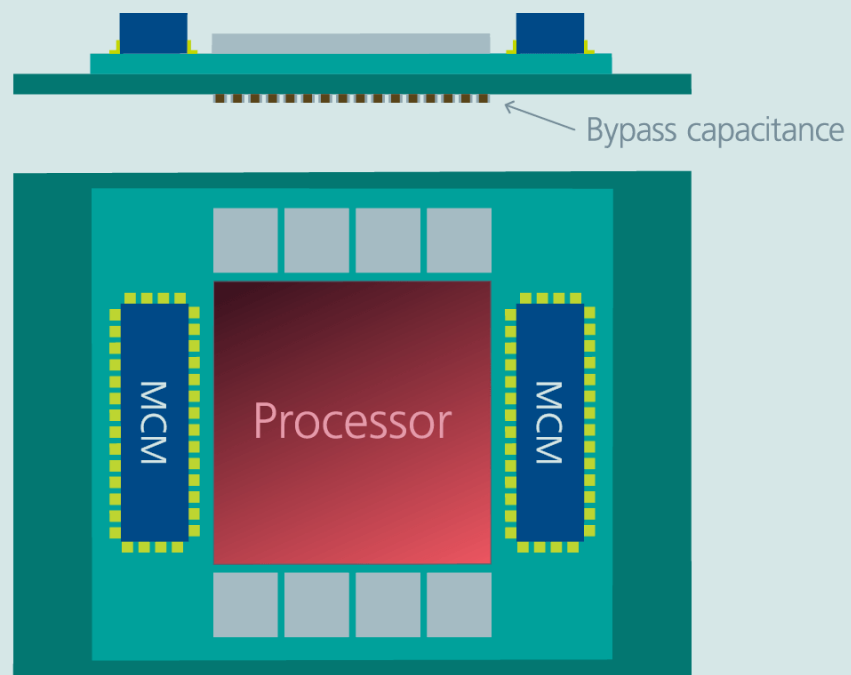
Factorized Power Architecture



Lateral Power Delivery

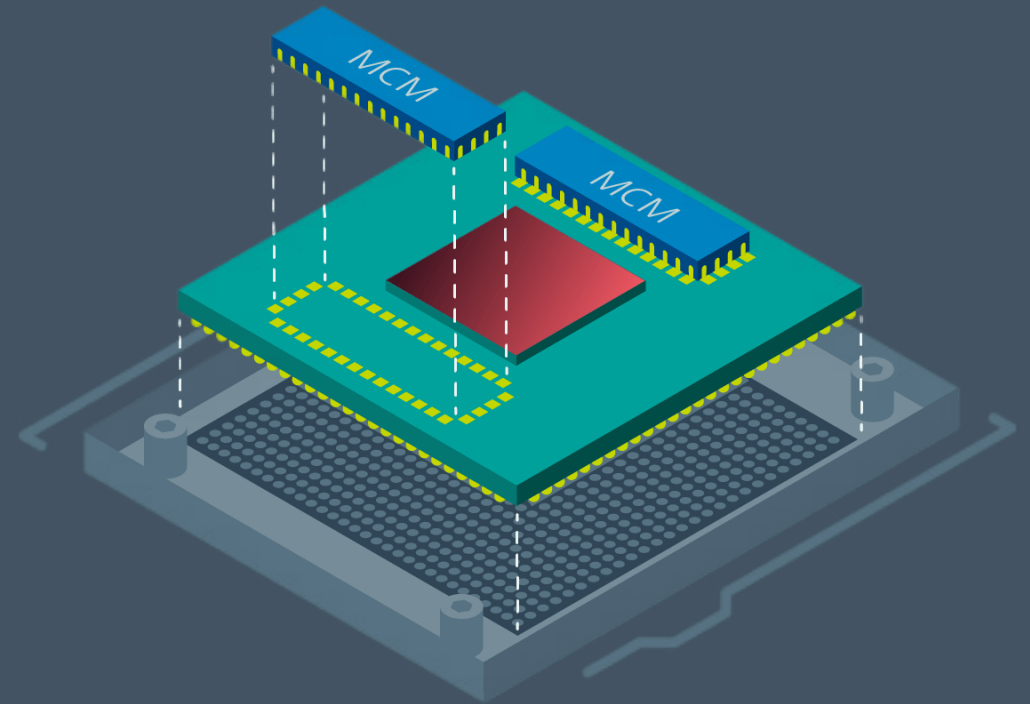


Lateral Power Delivery



Lateral Power Delivery

- Current Multipliers (“MCMs”)
 - Current Multiplication (e.g. 64-to-1) close to processor
 - Typical interconnect resistance: $100\mu\Omega$ per processor side
- Example MCM module performance
 - Two 46 x 9 x 3.2mm devices
 - Provide 750A continuous and 1,400A peak

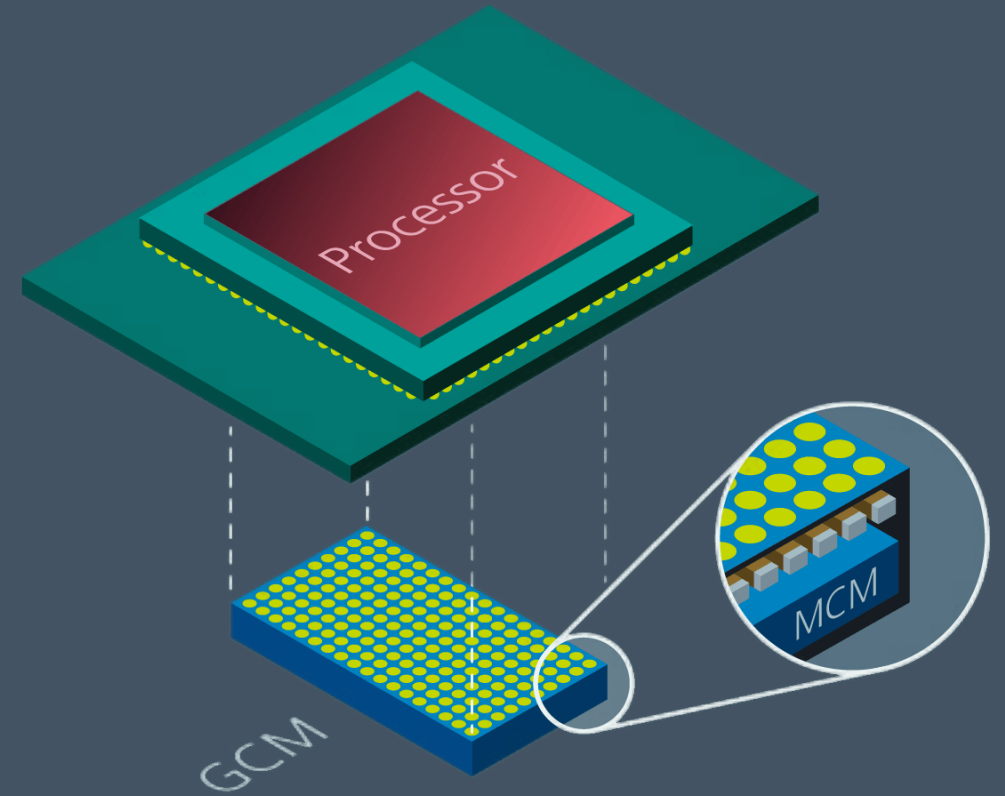
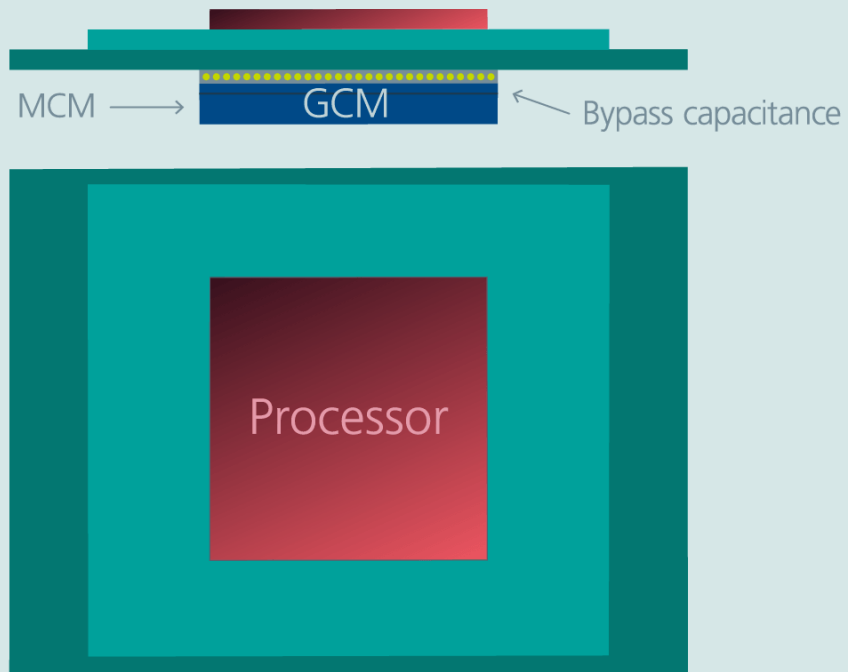


Performance loss analysis

	Vicor Lateral	Conventional
PDN resistance	50 $\mu\Omega$	400 $\mu\Omega$
PDN loss @ 500 Amps	12.5W loss 96.8% efficiency	100W 75% efficiency
PDN loss @ 1000 Amps	50W loss 93.75% efficiency	400W 50% efficiency

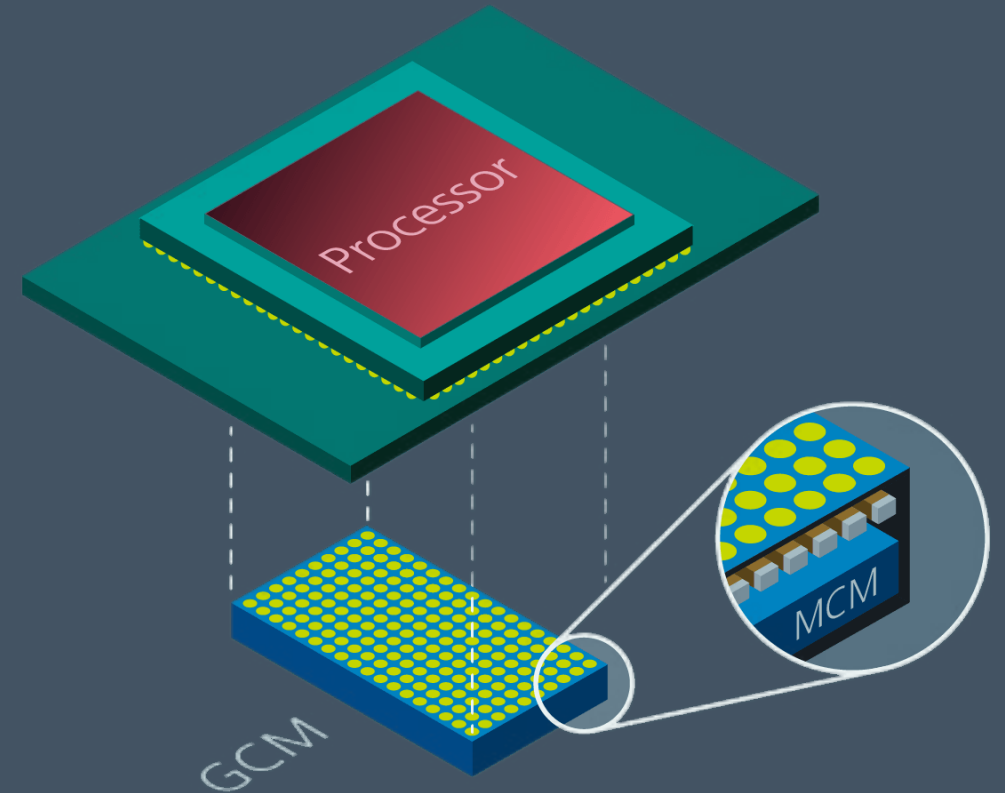
PDN Power Loss, due to circuit board copper resistance = I^2R

Vertical Power Delivery



Vertical Power Delivery

- Geared Current Multiplier (“GCM”)
 - Low interconnect resistance
 - Terminal pitch matched to processor (e.g., 1mm)
 - Processor perimeter unobstructed
- Power integrity
 - Bypass capacitors re-located within the GCM
 - Low GCM output inductance
 - Low noise ZCS/ZVS current multiplication



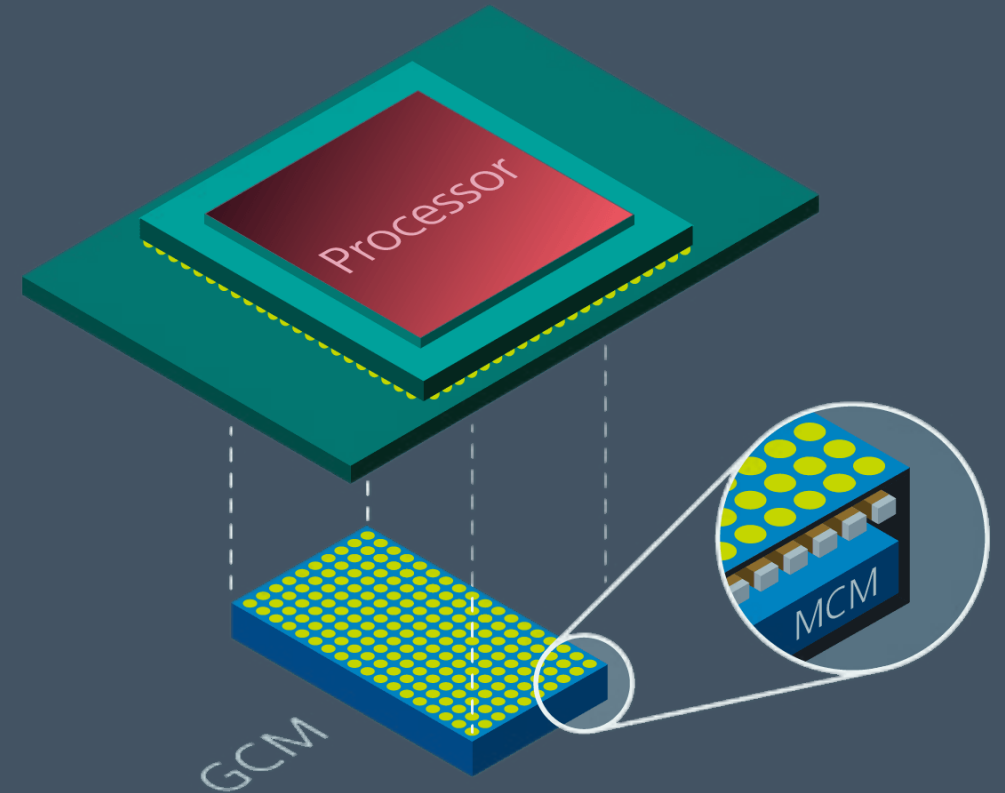
Performance loss analysis

	Vicor Vertical	Vicor Lateral	Conventional
PDN resistance	5 $\mu\Omega$	50 $\mu\Omega$	400 $\mu\Omega$
PDN loss @ 500 Amps	1.25W loss 99.7% efficiency	12.5W loss 96.8% efficiency	100W 75% efficiency
PDN loss @ 1000 Amps	5W loss 99.4% efficiency	50W loss 93.75% efficiency	400W 50% efficiency

PDN Power Loss, due to circuit board copper resistance = I^2R

Vertical Power Delivery

- Easy to cool
 - Vertical PDN loss much lower than Lateral PDN
 - Relatively low GCM heat density
- Example GCM module performance
 - One 33 x 30 x 4.1mm
 - Provides 1,000A continuous and 1,800A peak
- Also enables GCM mounted above processor for top side power delivery



Thank You